



VERIFICATION OF A TRANSLATION

I, the below name translator, hereby declare that:

My name and post office address are as stated below;

That I am knowledgeable in the English language and in the language in which the below identified international application was filed, and that I believed the English translation of the Japanese application 2003-321027 is a true and complete translation of the above-identified international application as filed.

I hereby declare that all statement made herein of my knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize validity of the application or any patent issued thereon.

Full name of the translator: Hitoshi Takahashi

Signature of the translator: *Hitoshi Takahashi*

Date: *May 14, 2007*

Post Office Address: 2nd floor, Fuji Building
5-11, Kudanminami 4-chome
Chiyoda-ku, Tokyo 102-0074
JAPAN



Claims:

1. A linear device including a gate electrode, a gate insulating region, a first semiconductor region, a second semiconductor region, and a third semiconductor region, in a radial direction within a cross section of a device region, characterized in

that said gate electrode located at a center; and said gate insulating region, said first semiconductor region with one or a plurality of opening(s), said second semiconductor region, said third semiconductor region, which are sequentially arranged around said gate electrode outwardly therefrom,

and that said third semiconductor region is arranged on said second semiconductor region which is contacted with said opening(s) of said first semiconductor region.

2. A linear device including a first region, a gate electrode, a gate insulating region, a first semiconductor region, a second semiconductor region, and a third semiconductor region, in a radial direction within a cross section of a device region, characterized in

that said first region located at a center; and said gate electrode, said gate insulating region, said first semiconductor region with one or a plurality of opening(s), said second semiconductor region, said third semiconductor region, which are sequentially arranged around said gate electrode outwardly therefrom,

and that said third semiconductor region is arranged on said second semiconductor region which is contacted with said

opening(s) of said first semiconductor region.

3. A linear device including a first semiconductor region, a second semiconductor region, a third semiconductor region, a gate insulating region, and a gate electrode, in a radial direction within a cross section of a device region, characterized in

that said first semiconductor region located at a center; and said second semiconductor region, said third semiconductor region, said gate insulating region, said gate electrode, which are sequentially arranged around said gate electrode outwardly therefrom,

and that said third semiconductor region is arranged to have one or a plurality of opening(s).

4. A linear device including a first region, a first semiconductor region, a second semiconductor region, a third semiconductor region, a gate insulating region, and a gate electrode, in a radial direction within a cross section of a device region, characterized in

that said first region located at a center; and said first semiconductor region, said second semiconductor region, said third semiconductor region, said gate insulating region, said gate electrode, which are sequentially arranged around said gate electrode outwardly therefrom,

and that said third semiconductor region is arranged to have one or a plurality of opening(s).

5. The linear device of any one of claims 1 through 4, wherein a plurality of circuit elements is arranged

continuously or intermittently along the longitudinal direction of the linear body.

6. The linear device of any one of claims 1 through 4, wherein a plurality of cross-sectional planes serving as circuit elements is arranged continuously or intermittently along the longitudinal direction of the linear body.

7. The linear device of any one of claims 1 through 6, wherein the cross-sectional shape thereof is circular, polygonal, star-shaped, crescent-shaped, petal-shaped, or character-shaped.

8. The linear device of any one of claims 1 through 7, wherein said first semiconductor region is a source region and said third semiconductor region is a drain region.

9. The linear device of any one of claims 1 through 7, wherein said first semiconductor region is a drain region and said third semiconductor region is a source region.

10. The linear device of any one of claims 2 or 4, wherein said first region is a space region, an insulating region, a semiconductor region, or an electroconductive region.

LINEAR DEVICE

TECHNICAL FIELD

[0001]

The present invention relates to a linear device comprising a MISFET formed in a linear body.

BACKGROUND ART

[0002]

It is possible to create various devices in arbitrary shapes, by utilizing linear devices each including a circuit element formed into a thread and by utilizing integrated circuits fabricated by such linear devices, since such linear devices and integrated circuits have resiliency and flexibility. FIG. 8 is a perspective view of a conventional linear device including a MISFET formed as a circuit element. The device includes a gate electrode 107 at a center of a cross section of the device, as well as a gate insulating region 108, a source region 110, a drain region 109, and a semiconductor region 112 sequentially formed outside the gate electrode. As shown in FIG. 9, a conventional MISFET device formed on a planar substrate is also known with a structure where application of control voltage to the gate electrode 114 controls electric current flowing through the semiconductor region 117 acting as a channel between the source region 116 and drain region 118.

DISCLOSURE OF THE INVENTION

Problem to be solved by the Invention

[0003]

The conventional MISFET shown in FIG. 8 has a channel length to be determined by a distance L between the source region 110 and drain region 109 along a surface of the insulating region 108. Production methods of linear MISFETs include one configured to simultaneously feed gel-like electroconductive or semiconductive polymer materials acting as starting materials of a semiconductor region, a source region, and a drain region, respectively, into a die for controlling a cross-sectional shape of a circuit element, in a manner to eject the polymer materials from the die into a linear form which is

to be subsequently solidified. This method is problematic in insufficient uniformity and insufficient reproducibility of channel lengths, due to non-uniformity of viscosities, thermal expansion coefficients, and the like of gel-like polymer materials, respectively. Further, although there exists another production method for forming a gate electrode/gate insulating region, with a source region, a drain region, and an insulating region formed on its surface as separate linear bodies, respectively, and for bundling up the linear bodies to thereby form the structure shown in FIG. 9, it fails to attain a sufficiently high precision, due to dependency of a channel length on positional accuracies in a bundling procedure. As such, about $1\mu\text{m}$ has been a limitation of downsizing of a channel length in any one of the above situations, and it has been difficult to improve high-frequency characteristics, degree of integration, and the like by a downsized channel length.

[0004]

The other conventional MISFET shown in FIG. 9 has a channel length to be determined by the thickness of a semiconductor region 119. The thickness of the semiconductor region 119 can be controlled well when the region 119 is formed by spin coating, or the like, therefore the channel length of the MISFET can also be controlled with high accuracy and good reproducibility. Further, the controllability and the accuracy of the thickness are better than those of lateral patterning. It is possible to form MISFETs shown in Fig. 9 with channel length less than or equal to $1\mu\text{m}$. However, when an integrated circuit is

fabricated using MISFETs shown in Fig.9, which are formed on a planer substrate, there is a problem that the production yield improvement of such a integrated circuit will be difficult when the size of the integrated circuit increases, because even only one defect among many devices of the integrated circuit will cause malfunction of the whole integrated circuit.

Means for solving the Problem

[0005]

There is provided a linear device comprising a MISFET having a structure including, in a radial direction within a cross section of a device region: a film-like semiconductor region serving as a channel region interposed between a source region and a drain region. A control voltage is applied to the semiconductor region through a gate insulating region to control current which flows between the source region and the drain region.

Effect of the Invention

[0006]

(1) Since the MISFET has a structure including the semiconductor region serving as the channel region between the source region(s) and the drain region (s) in a radial direction within a cross section of the device region, the channel has a length to be determined by the film thickness of the semiconductor region. This enables downsizing, and improvement of reproducibility and uniformity, of the channel length.

(2) In case an integrated circuit is fabricated by

assembling a plurality of linear devices, it is possible to use only non-defective linear devices selected by testing, or to replace defective linear devices by non-defective ones after assembling the integrated circuit. Therefore, it is possible to improve fabrication yield for a very large scale integrated circuit without special strict process control.

(3) In case that a plurality of MISFETs are arranged intermittently along the longitudinal direction of the linear body, a circuit with a plurality of MISFETs with a common gate electrode can be easily formed if a linear gate electrode is arranged at the center of a linear body. Similarly, a circuit with a plurality of MISFETs with a common source region can be easily formed if a linear source region is arranged at the center of a linear body. And also, a circuit with a plurality of MISFETs with a common drain region can be easily formed if a linear drain region is arranged at the center of a linear body. Further, a plurality of MISFETs can be easily electrically separated if a linear isolating region is arranged at the center of a linear body.

BEST MODE FOR CARRYING OUT THE INVENTION

[0007]

FIG. 7 is a perspective view of a linear device according to a concrete example of the present invention. The linear device according to a concrete example of the present invention is a MISFET which comprises, within a cross section of the linear device: a gate electrode 101 located at a center; and a gate

insulating region 102, source regions 103, a semiconductor region 104, and a drain region 105. In case an N-type MISFET is taken as an example, as shown in Fig. 7, there is provided a linear device comprising a MISFET having a structure including, in a radial direction within a cross section of a device region: a P-type semiconductor region 104 serving as a channel region interposed between a N-type source region 103 and a N-type drain region 105, and a gate electrode 101 arranged on a insulating region 102 adjacent to a semiconductor region 104. The source region 103 is arranged to have at least one opening, and the drain region 105 is arranged over the opening. When positive voltage higher than a threshold voltage is applied to the gate electrode 101 relative to the potential of the semiconductor region 104, electrons will be induced in the semiconductor region 104 between a source region 103 and a drain region 105, thereby enhancing conductivity between the source region 103 and the drain region 105, then currents from the source region 103 to the drain region 105 can be controlled by the voltage applied to the gate electrode 101.

[0008]

The MISFET shown in Fig. 7 has a structure for interposing a semiconductor region serving as a channel region between a source region(s) 103 and a drain region(s) 105 in a radial direction of a cross section of a device region, in a manner to determine a channel length by the film thickness of the semiconductor region 104. This enables downsizing, and improvement of reproducibility and uniformity, of the channel

length.

[0009]

Although the concrete example of the present invention shown in Fig.7 has been described about the situation where the number of dividedly provided source regions or drain regions is 4, the effects of the present invention can be equally obtained even in a case of a MISFET having dividedly provided source regions or drain regions the number of which is 2, 3, 5, ..., and the like differently from the above.

[0010]

And also, the effects of the present invention can be equally obtained even in a case when the central region of the linear device (gate electrode 101 for the embodiment shown in Fig.7) has a region or regions in its center such as a space region, an insulating region, a semiconductor region, or electroconductive region. In a case a linear device has a electroconductive region made of an electroconductive organic polymer material in its center, it is desirable to mix fullerene or endhedral fullerene therewith for the electroconductive material. Desirable as fullerene is C_n ($n=60$ to '80). Desirable as a contained atom(s) of endhedral fullerene is Na, Li, H, N, or F.

EMBODIMENT

[0011]

(Linear Device)

FIG. 1 is a perspective view of a linear device according

to a first embodiment of the present invention. The linear device according to the first embodiment of the present invention comprises, within a cross section of the linear device: a gate electrode 1 located at a center; and a gate insulating region 2, source regions 3, a semiconductor region 4, and a drain region 5, which are sequentially arranged around the gate electrode outwardly therefrom. Insulating region 6 is formed around the linear device for the protection of the linear device. In a linear device shown in FIG.1, a plurality of circuit devices is formed consecutively in the longitudinal direction of the linear device.

[0012]

FIG. 2 is a perspective view of a linear device according to a second embodiment of the present invention. Similar to the first embodiment, the linear device according to the second embodiment of the present invention comprises, within a cross section of the linear device: a gate electrode 1 located at a center; and a gate insulating region 2, source regions 3, a semiconductor region 4, and a drain region 5, which are sequentially arranged around the gate electrode outwardly therefrom. Insulating region 6 is formed around the linear device for the protection of the linear device. As the material for forming gate electrode 1, both organic electroconductive material and inorganic electroconductive material can be used. In a linear device shown in FIG.2, a plurality of circuit devices are formed intermittently in the longitudinal direction of the linear device, and the linear device is divided into MISFET

region 21, drain electrode region 22, separation region 23, and MISFET region 24.

[0013]

FIG. 3(a) is a cross-sectional view of a linear device at the MISFET region 21 of the linear device shown in FIG. 2. Arranged sequentially around and outwardly from a gate electrode 1 made of electroconductive polymer at a center, are a gate insulating region 82 made of insulating polymer, source regions 3 made of N-type semiconductive polymer, a semiconductor region 4 made of P-type semiconductive polymer, a drain region 5 made of N-type semiconductive polymer. When positive voltage is applied to the gate electrode 1 relative to the potential of the semiconductor region 4, electrons will be induced in the semiconductor region 4 adjacent to the gate insulating region 1, thereby enhancing conductivity between the source region 3 and the drain region 5.

[0014]

FIG. 3(b) is a cross-sectional view of a linear device at the drain region 22 of the linear device shown in FIG. 2. A drain electrode 7 made of electroconductive polymer is formed around the semiconductor region 4, and is electrically connected to the drain region 5.

[0015]

FIG. 3(c) is a cross-sectional view of a linear device at the separation region 23 of the linear device shown in FIG. 2. In the separation region 23, a drain region 5 is not placed, and a separation region 8 made of insulating polymer is formed

around the semiconductor region 4.

[0016]

A linear device shown in Fig. 2 is comprised of a plurality of MISFETS which have a common gate electrode, a common source region. And drain regions are formed separately for each MISFET. It is also possible to form gate electrodes and source regions separately for each MISFET. And also, it is possible to arrange for a plurality of MISFETS to have a common drain region. Further, it is apparent that MISFETS function normally and the same effect of the invention can be obtained as a linear device shown in Fig. 2 when source regions and drain regions are exchanged in the aforementioned linear devices.

[0017]

Fig. 4 is a perspective view of a linear device according to a third embodiment of the present invention. A MISFET according to the third embodiment of the present invention comprises, within a cross section of the linear body: a source region 31 located at a center; a semiconductor region 32, drain regions 33, a gate insulating region 34, a gate electrode 35, which are sequentially arranged around the insulating region outwardly therefrom. A plurality of drain regions 53 is located with opening(s) in a radial direction within a cross section of the linear body. Further, an insulating region 36 is arranged around the linear body for a surface protection. MISFETS according to the first and the second embodiment of the present invention have a device structure to control the electroconductivity of a semiconductor region between a source

region and a drain region which are arranged at the outer part of the linear body by the potential of a gate electrode arranged inside the linear body. On the other hand, MISFETs according to the third embodiment of the present invention have a device structure to control the electroconductivity of a semiconductor region between a source region and a drain region which are arranged inside the linear body by the potential of a gate electrode arranged at the outer part of the linear body. In case that a plurality of MISFETs is arranged intermittently along the longitudinal direction of the linear body, a linear device with common source region and electrical separation among the gates, and the drains of each MISFETs can be easily formed by arranging a linear insulating region at the center of the linear body as a structural support of the linear body. Generally speaking, circuits based on MISFET technology are comprised of many devices with common source. Wiring structure will be simplified when an integrated circuit of such a type is formed using linear devices with common source region. Further, it is apparent that MISFETs function normally when source regions and drain regions are exchanged in the aforementioned linear devices.

[0018]

Fig. 5 is a perspective view of a linear device according to a fourth embodiment of the present invention. A MISFET according to the fourth embodiment of the present invention, unlike a MISFET according to the third embodiment of the present invention, an insulating region is placed at the center of the

linear body. The MISFET according to the fourth embodiment of the present invention comprises, within a cross section of the linear body: an insulating region 57 located at a center; a source region 51, a semiconductor region 52, drain regions 53, a gate insulating region 54, a gate electrode 55, which are sequentially arranged around the insulating region outwardly therefrom. A plurality of drain regions 53 is located with opening(s) in a radial direction within a cross section of the linear body. Further, an insulating region 56 is arranged around the linear body for a surface protection. In case that a plurality of MISFETs is arranged intermittently along the longitudinal direction of the linear body, electrical separation among the gates, the drains, the sources, and the substrates of each MISFETs can be easily implemented by arranging a linear insulating region at the center of the linear body as a structural support of the linear body. Organic insulating materials, or inorganic insulating materials can be used for an insulating region 57.

[0019]

FIG. 6(a) is a cross-sectional view of a linear device at the MISFET region 61 of the linear device shown in FIG. 5. The MISFET shown in Fig. 6(a) comprises, within a cross section of the linear body: an insulating region 57 located at a center; a source region 51 made of N-type semiconductive polymer, a semiconductor region 52 made of P-type semiconductive polymer, drain regions 53 made of N-type semiconductive polymer, a gate electrode 55 made of electroconductive polymer, which are

sequentially arranged around the insulating region outwardly therefrom. When positive voltage is applied to the gate electrode 55 relative to the potential of the semiconductor region 52, electrons will be induced in the semiconductor region 52 adjacent to the surface of the gate insulating region 54, thereby enhancing conductivity between the source region 51 and the drain region 53.

[0020]

FIG. 6(b) is a cross-sectional view of a linear device at the gate electrode region 62 of the linear device shown in FIG. 5. An electrode region made of electroconductive polymer is formed around the gate electrode 55.

[0021]

FIG. 6(c) is a cross-sectional view of a linear device at the separation region 63 of the linear device shown in FIG. 5. In the separation region 63, a gate electrode 55, a drain region 53, and a source region 51 are not placed, and a separation region 58 made of insulating polymer is formed around the isolation region 57.

[0022]

FIG. 6(d) is a cross-sectional view of a linear device at the drain electrode region 64 of the linear device shown in FIG. 5. A drain electrode 59 made of electroconductive polymer is formed around the drain region 53, and is electrically connected to the drain region 53.

[0023]

(Shape of Linear Device)

It is desirable that the linear devices of the present invention are each 10mm or less, preferably 5mm or less in outer diameter. 1mm or less is desirable, and 10 μ m or less is more desirable. It is also possible to attain 1 μ m or less, and even 0.1 μ m or less.

[0024]

In case of eventually forming an extrafine linear body having an outer diameter of 1 μ m or less by discharging it from a hole of a die, there may be caused clogging of the hole, breakage of a thread-like body, or the like. In such a case, there are firstly formed linear bodies of respective regions. Next, these linear bodies may be regarded as many islands, respectively, which are then each surrounded at a periphery (sea) thereof by a meltable matter and subsequently bundled up by a funnel-shaped nozzle followed by discharge into a single linear body. Increasing island components and decreasing sea components enables formation of an extremely fine linear body device. As another method, it is possible to once prepare a thick linear body device, and to subsequently extend it in a longitudinal direction thereof. Alternatively, it is also possible to place a molten starting material(s) into a jet stream to thereby melt blow it into an extrafine one.

[0025]

Meanwhile, it is possible to attain an aspect ratio of an arbitrary value by extrusion forming. 1,000 or more is desirable in case of a thread shape by spinning. 100,000 or more is also possible, for example. In case of usage after

cutting, 10 to 10,000, 10 or less, 1 or less, and 0.1 or less is possible, for small units of linear devices.

[0026]

The linear device is not particularly limited in cross-sectional shape. For example, it may be circular, polygonal, star-shaped, and so on. It may be a polygonal shape having a plurality of apex angles each defining an acute angle. In turn, it is possible that respective regions each have an arbitrary cross section. Depending on a type of device, it is desirable to provide a region layer in a polygonal shape having apex angles each defining an acute angle, in case of intending a wider contacting area between the region layer and a neighboring one. Note that it is possible to easily realize a desired cross-sectional shape, by preparing an extrusion die in the desired shape. In case that an outermost layer is in a star shape or in a shape having apex angles each defining an acute angle, it is possible to fill an arbitrary material(s) into spaces between neighboring apexes such as by dipping after extrusion forming, thereby changing a property of a device depending on the usage thereof.

[0027]

In case a semiconductor region needs impurity doping, it is possible to mix the dopant in the material in a molten state, and it is also possible to dope impurity in a linear body in the vacuum chamber by ion implantation, for example, after extrusion forming and transferring as linear body in the vacuum chamber. When the semiconductor region is formed inside the

linear body, implantation energy will be adjusted to control the depth of the implanted region.

[0028]

In aforementioned production example, a linear body of the present invention is formed as one body by extruding devices with a plurality of layers. A linear device of the present invention can also be formed by extruding the main part of the linear device, then forming coated layer(s) on the main part of the linear body by appropriate method.

[0029]

(Material of Linear Device)

As an electroconductive material and a semiconductor material for forming the linear device of the present invention, it is desirable to adopt an electroconductive polymer. Usable as an electroconductive polymer are polyacetylenes, polyacenes, (olygoathenes), polythiazyl, polythiophenes, poly(3-alkylthiophene), oligothiophene, polypyrrole, polyaniline, polyphenylenes, and the like. It is preferable to select one(s) of them as an electrode or semiconductor layer in consideration of an electrical conductivity and the like.

[0030]

Further, preferably used as an organic semiconductor are polyparaphenylenes, polythiophenes, poly(3-methylthiophene), and the like.

Moreover, usable as a material of a source/drain region, is the above-described semiconductor material including a dopant mixed therewith.

For establishment of an N-type semiconductor, it is enough to adopt alkali metal (Li, Na, K), $\text{AsF}_5/\text{AsF}_3$, ClO_4^- as a dopant, for example.

[0031]

(Production Apparatus and Production Method)

FIG. 10 is a front view of a production apparatus of the linear device of the present invention.

Reference numeral 11 designates an extrusion apparatus having starting material reservoirs 12, 13, 14 for holding therein starting materials in molten states, dissolved states, or gel states so as to constitute a plurality of regions, respectively. Although the three starting material reservoirs are presented in the example shown in FIG. 10, it is possible to appropriately provide starting material reservoirs correspondingly to a configuration of a linear device to be produced.

The starting material reservoir 12 contains a starting material therein to be fed to a die 15. The die 15 is formed with ejection holes commensurating with a cross section of a linear device to be produced. To be collectively ejected from the ejection holes is a linear body which is wound up by a roller 17 or which is delivered to a next process as required in the linearized state.

A production apparatus with a structure shown in FIG.10 is used for producing linear devices with a structure shown in FIG.1 and FIG.2.

[0032]

The starting material reservoirs 12, 13, 14 hold therein a gate electrode material, a gate insulating region material, a source material, a drain material, and a semiconductor material in a molten or dissolved state, or a gel state, respectively. Meanwhile, the die 15 is formed with holes communicated with the material reservoirs, respectively.

[0033]

As shown in a plan view of FIG. 11, the die 15 is formed at its central part with a plurality of holes for ejecting the gate electrode material. Outwardly and peripherally formed around the holes is a plurality of holes for ejecting the gate insulating region material. Further, outwardly and peripherally formed around the holes are a plurality of holes for ejecting the source material, drain material, and semiconductor material, respectively. However, it is enough in the die 20 that the arrangement of the pluralities of holes for ejecting the materials corresponding to a circuit region is appropriately set correspondingly to a cross-sectional structure of a linear device to be actually produced, and it is not absolutely required that holes for ejecting a gate electrode material are arranged centrally.

[0034]

The starting materials in a molten or dissolved state, or a gel state are fed from the starting material reservoirs into the die 20, ejected from the die through the holes, and then solidified. Pulling an end of the solidified matter forms a continuous and linear light emitting device in a thread shape.

[0035]

The linear device is wound up by the roller 17. Alternatively, the solidified matter in the thread shape is delivered to the next process as required. For example, it is possible to inject oxygen ions at a doping treatment part 18 followed by heating, thereby forming an insulating separation region. And it is possible to form drain extraction electrode 7 by conducting coating of an electroconductive polymer at an electrode formation treatment part 19. To contact a drain region 5 with a drain extraction electrode 7, there is provided a treatment part for removing a part of a semiconductor region 4 by a method such as mechanical working, etching, or the like before formation of the electrode. And also, it is possible to provide an insulating material coating treatment part which is not shown in FIG.10. Then each MISFET formed on a linear device shown in FIG.5 can be electrically isolated by removing part of gate electrode 55, gate insulating region 54, drain region 53, semiconductor region 52, and source region 51 by a method such as mechanical working, etching, or the like, so as to leave insulating region 57 unremoved between each two adjacent MISFETs, then coating insulating material around the insulating region 57. This isolation method is practicable for a linear device shown in FIG.2, if isolation region is formed at the center of the device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0036]

[FIG. 1] A perspective view of a linear device of the present invention according to a first embodiment.

[FIG. 2] A perspective view of a linear device of the present invention according to a second embodiment.

[FIG. 3] (a) is a cross-sectional view of a linear device at the MISFET region 21 shown in FIG. 2. (b) is a cross-sectional view of a linear device at the drain extraction electrode region 22 shown in FIG. 2. (c) is a cross-sectional view of a linear device at the separation region 23 shown in FIG. 2.

[FIG. 4] A perspective view of a linear device of the present invention according to a third embodiment.

[FIG. 5] A perspective view of a linear device of the present invention according to a fourth embodiment.

[FIG. 6] (a) is a cross-sectional view of a linear device at the MISFET region 61 shown in FIG. 5. (b) is a cross-sectional view of a linear device at the gate extraction electrode region 62 shown in FIG. 5. (c) is a cross-sectional view of a linear device at the drain extraction electrode region 64 shown in FIG. 5.

[FIG. 7] A perspective view of a linear device of the present invention.

[FIG. 8] A perspective view of a conventional linear device.

[FIG. 9] A cross-sectional view of a conventional circuit device formed on a planar substrate.

[FIG. 10] A front view of a production apparatus of the

linear device of the present invention.

[FIG. 11] A plan view of a die to be used for production of the linear device of the present invention.

Explanation of reference numerals

[0037]

1, 101, 107, 35, 55	gate electrode
2, 102, 108, 34, 54	gate insulating region
3, 103, 110, 31, 51	source region
4, 104, 112, 32, 52	semiconductor region
5, 105, 109, 33, 53	drain region
6, 106, 36, 56, 57	insulating region
7, 59	drain extraction electrode
8, 58	separation region
21, 24, 41, 45, 61, 65	MISFET region
22, 44, 64	drain extraction electrode region
23, 43, 63	separation region
42, 62	gate electrode region
11	extrusion apparatus
12	starting material 1 reservoir
13	starting material 2 reservoir
14	starting material 3 reservoir
15, 20	die
16	linear device
17	roller
18	doping treatment part

19	electrode formation
	treatment part
113	substrate
114	gate electrode
115	gate insulating region
116	source region
117	semiconductor region
118	drain region
119	insulating region

ABSTRACT

In a linear MISFET having a feature of resiliency and flexibility and capable of being fabricated into an integrated circuit in an arbitrary shape, there has been conventionally adopted a structure including a source region and drain region arranged in parallel. However, since a channel length of the MISFET for determining the electric characteristics thereof is determined by a distance between the source region and the drain region across a cylindrical gate insulating region, it has been difficult to downsize the channel length or improve reproducibility thereof, for example. The present invention provides a MISFET having a structure including a semiconductor region serving as a channel region interposed between a source region(s) and a drain region(s). Application of control voltage to the semiconductor region through the gate insulating region, controls electric current flowing between the source

region(s) and drain region(s). The channel length is determined by a film thickness of the semiconductor region, thereby exemplarily enabling downsizing and improvement of reproducibility, of the channel length.



FIG. 1

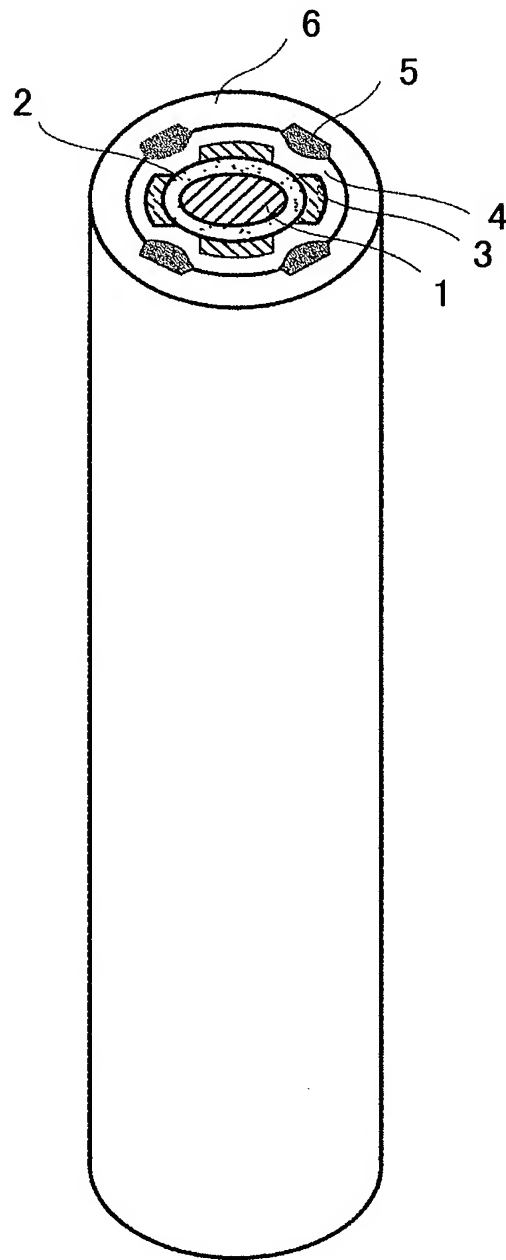


FIG. 2

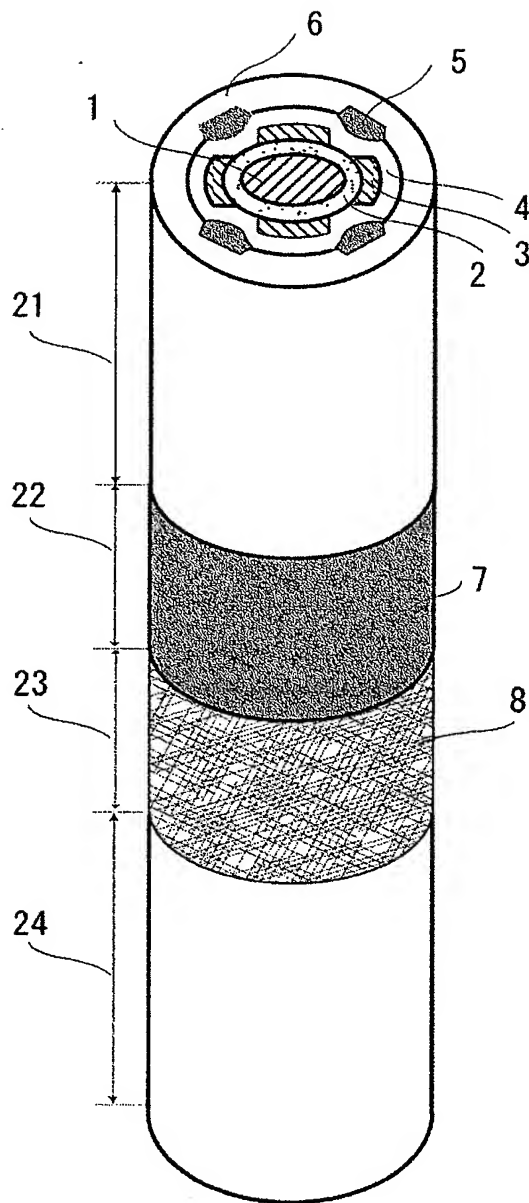


FIG. 3

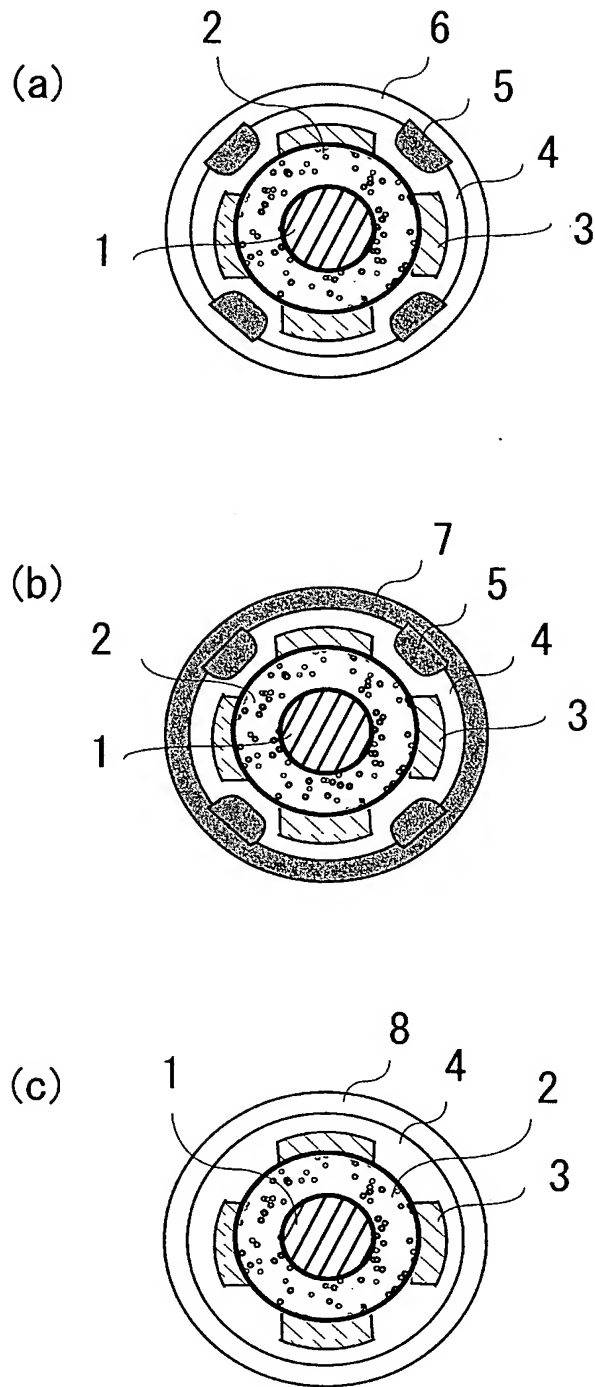




FIG. 4

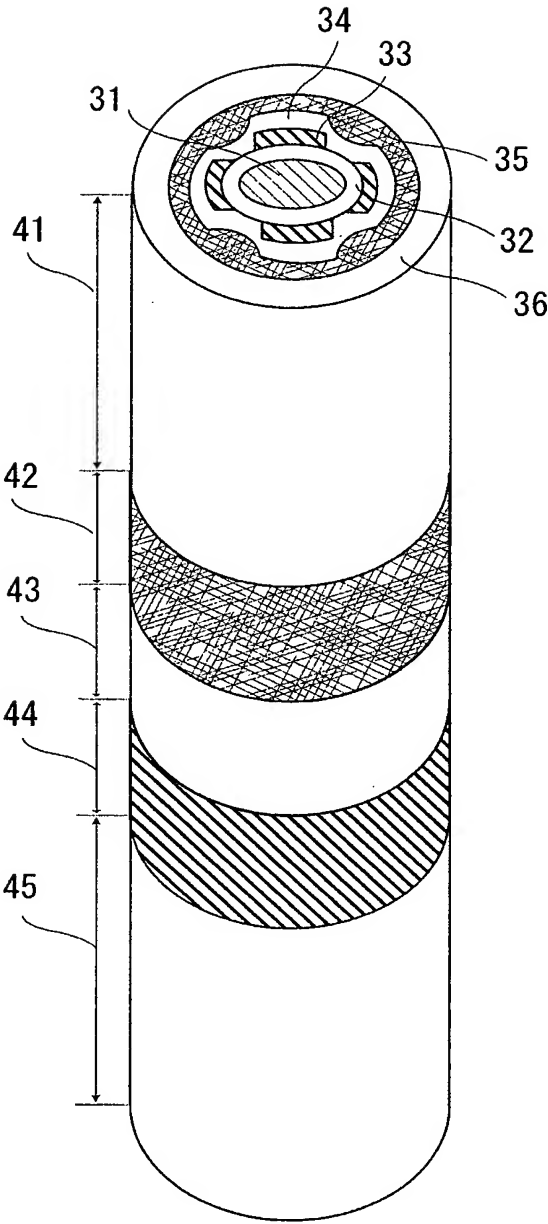




FIG. 5

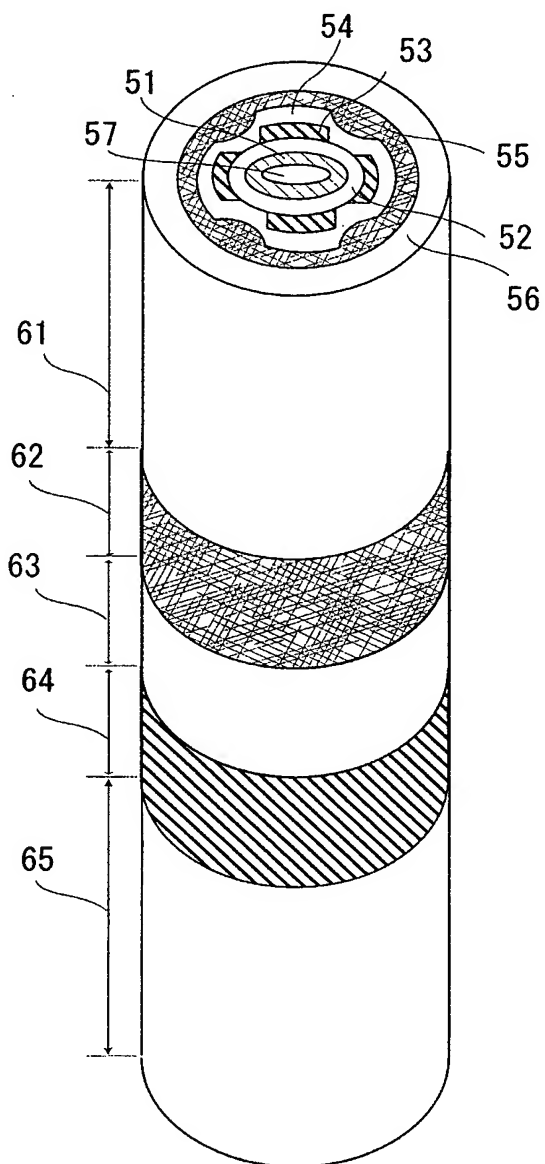


FIG. 6

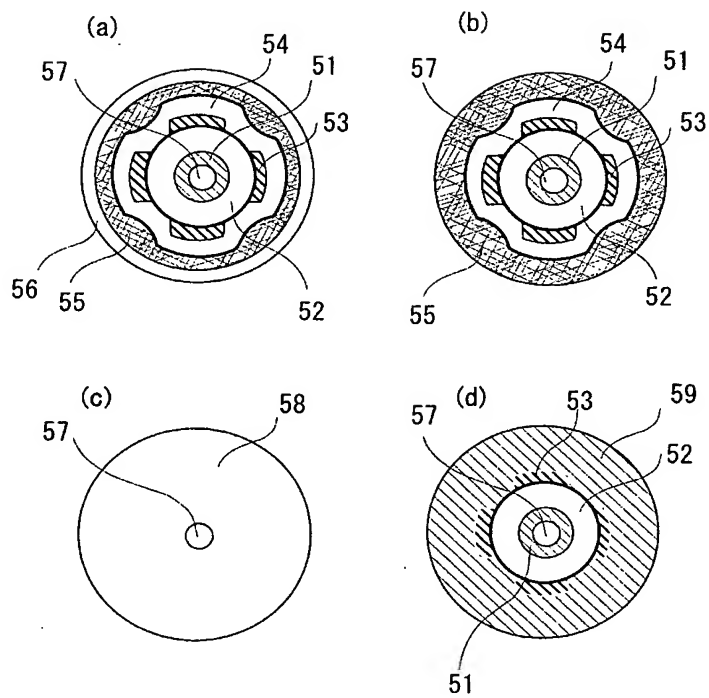


FIG. 7

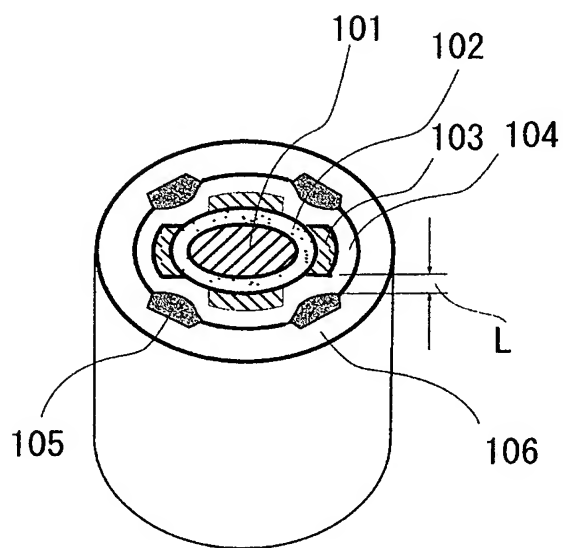


FIG. 8

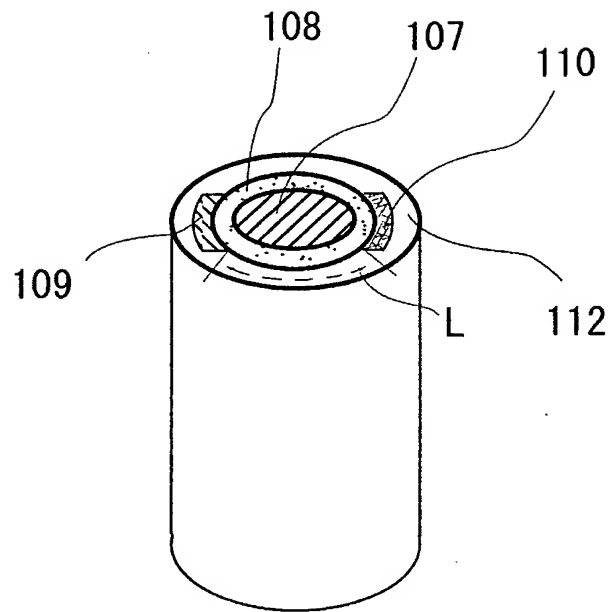


FIG. 9

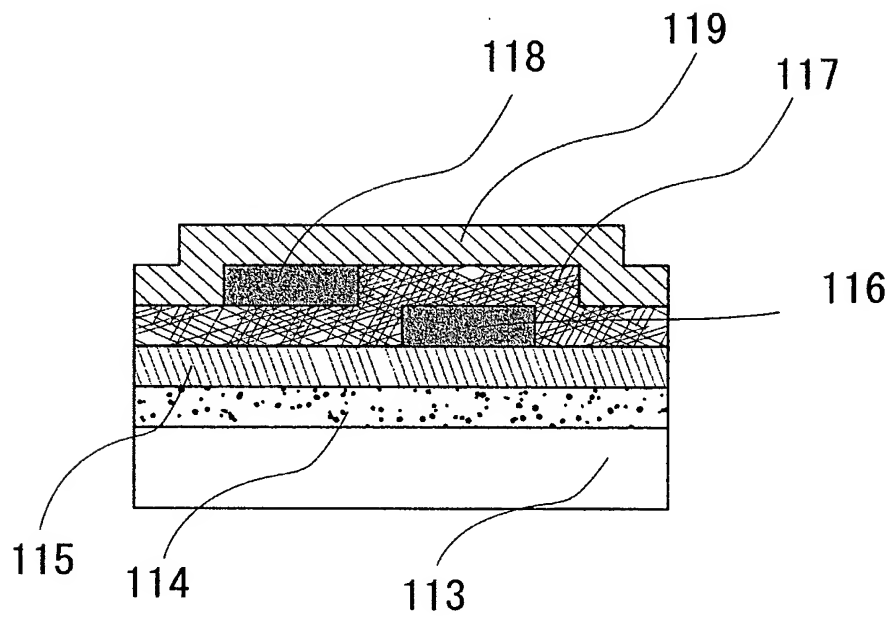


FIG. 10

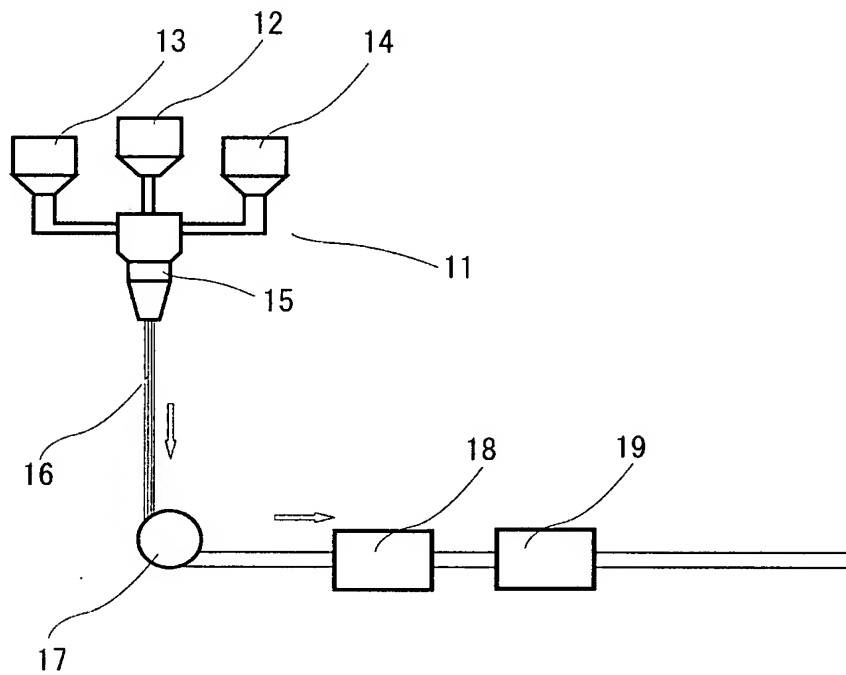


FIG. 11

